



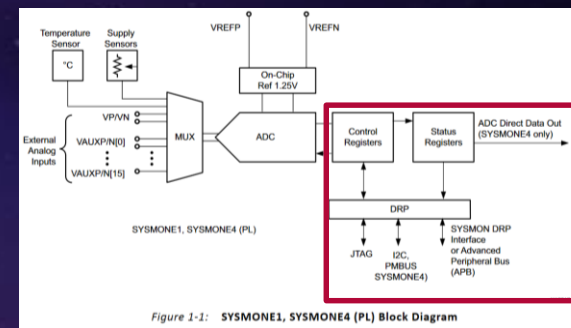
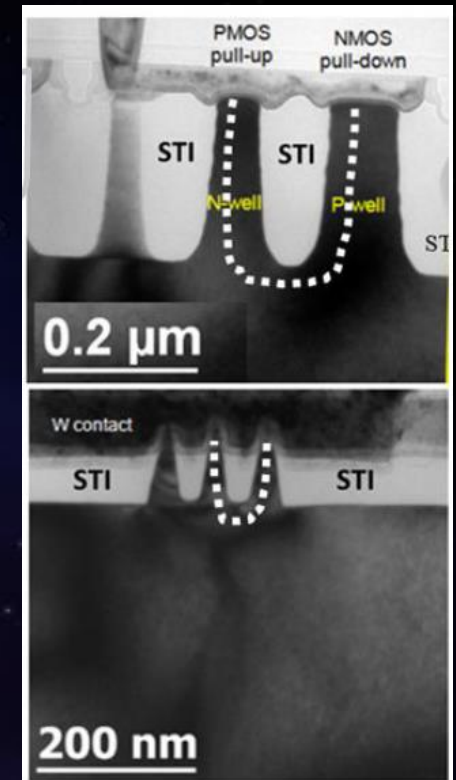
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UltraScale+ 16nm SEL Experiments Review

November 17th, 2017

16nm US+ SEL & SEU Event Rates

- TSMC 16nm FinFET technology has significantly lower SEU rate than previous nodes, as anticipated by earlier test chips
- However, TSMC 16nm FinFET technology has shown increased sensitivity to SEL, due to shallower STI¹
- SEL was not observed on previous TSMC planar technology nodes in proton testing
- Three circuits in product identified as SEL susceptible
 - Processing System (PS) System Monitor Circuit
 - Powered by V_{CC_PSAUX}
 - Programmable Logic (PL) System Monitor Circuit
 - Powered by V_{CCAUX}
 - HP-IO Auxiliary Circuits
 - Powered by V_{CCAUX_IO}



¹ “Single Event Latch-Up: Increased Sensitivity from Planar to FinFET” J. Karp, M. J. Hart, P. Maillard, Xilinx, Inc.; G. Hellings, D. Linten, IMEC; IEEE NSREC 2017

Deep PWell implant Experiment

➤ 16nm UltraScale+ Product w/ modified process

- Additional Deep Pwell implant

➤ Crocker Nuclear Laboratory Proton facility (CNL)

- 64 MeV mono-energetic Proton Beam
- Test @ 100°C & equivalent to 40 million years of radiation applied (relative to NYC sea level)

➤ Lawrence Berkeley Nuclear Lab Heavy Ion facility (LBNL)

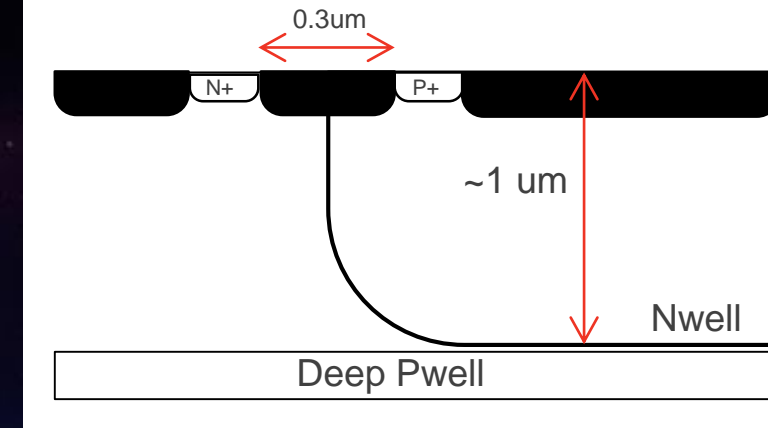
- 10 MeV ion cocktail w/ LET range 1 – 60 MeV.cm²/mg

➤ Improvement in SEL observed in both cases; does not meet space level needs

- Threshold SEL LET improved ~ 2X; yet still too low for Space applications < 30 MeV.cm²/mg
- SEL event rate improved by ~10X

➤ Conclusion

- Process experiment inadequate to solve SEL



Deep NWell Experiment

➤ 16nm Test Vehicle w/ Deep Nwell Design modules

- Deep Nwell isolation placed under known SEL locations

➤ Crocker Nuclear Laboratory Proton facility (CNL)

- 64 MeV mono-energetic Proton Beam
- Test @ 100°C & equivalent to 40 million years of radiation applied (relative to NYC sea level)

➤ Lawrence Berkeley Nuclear Lab Heavy Ion facility (LBNL)

- 10 MeV ion cocktail w/ LET range 1 – 60 MeV.cm²/mg

➤ SEL performance improvement observed in both cases; does not meet space level needs

- SEL Threshold LET increased by ~ 2X; yet still too low for Space applications < 30 MeV.cm²/mg
- SEL event rate improved by 3 – 4X

➤ Conclusion

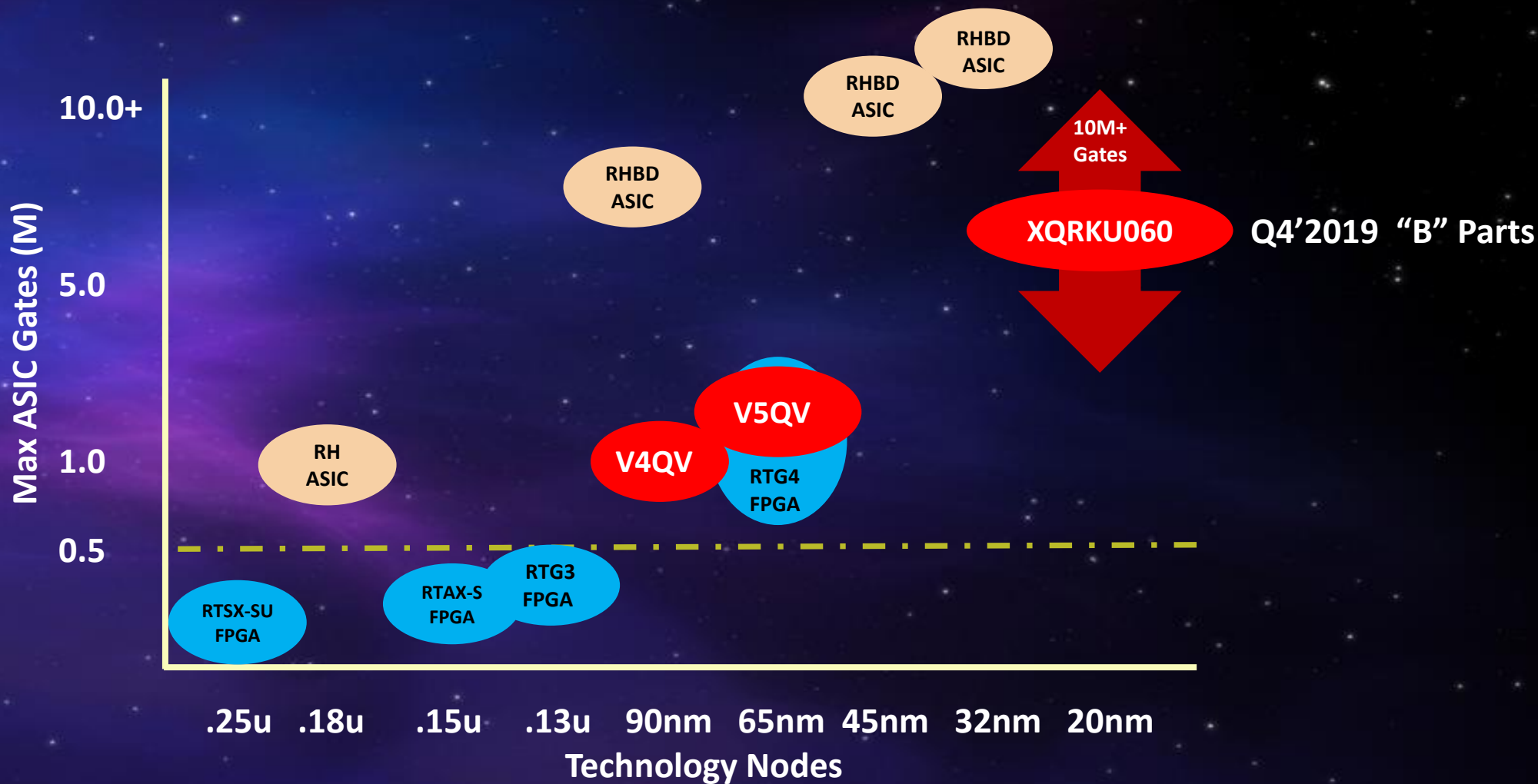
- Design / Process experiment inadequate to solve SEL



XQR Kintex UltraScale KU060 for Space Applications

Daniel Elftmann
Space System Architect
October 20th, 2017

Space FPGA/ASIC Marketplace



Microsemi

RH-ASIC

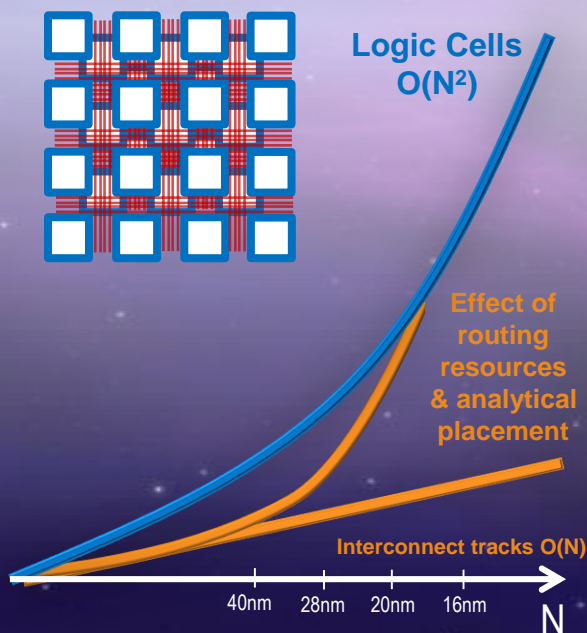
Xilinx

UltraScale Re-Architects the Core

Highest Utilization at Maximum Performance

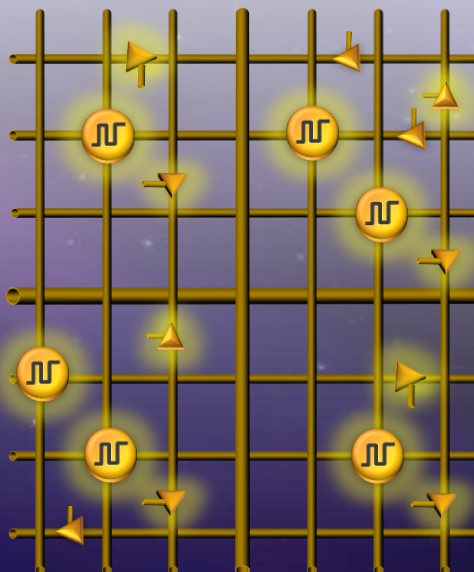
Next Generation Routing

- Re-designed routing architecture
- 2X routing, agile switching
- Co-Optimized with Vivado



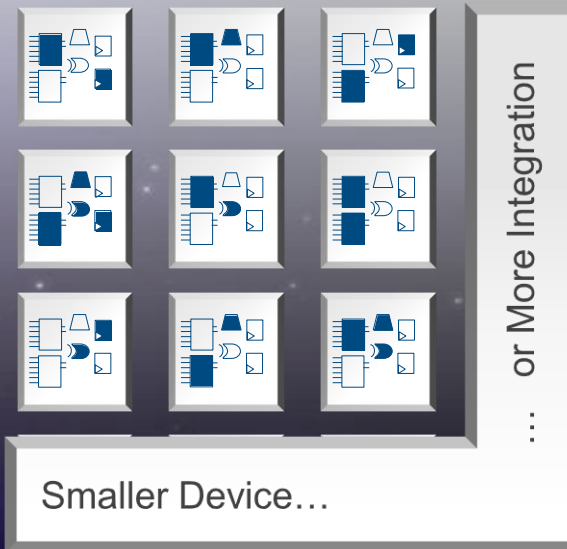
ASIC-Like Clocking

- Regional, segmented structure
- Flexible clock placement
- Scales w/density to balance skew



System Logic Cells

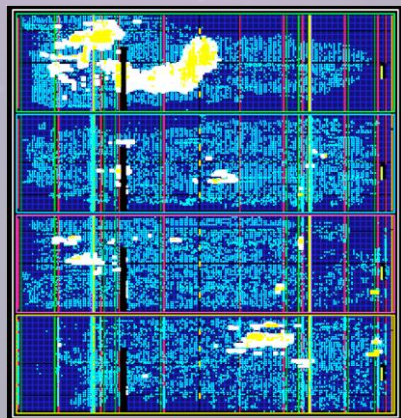
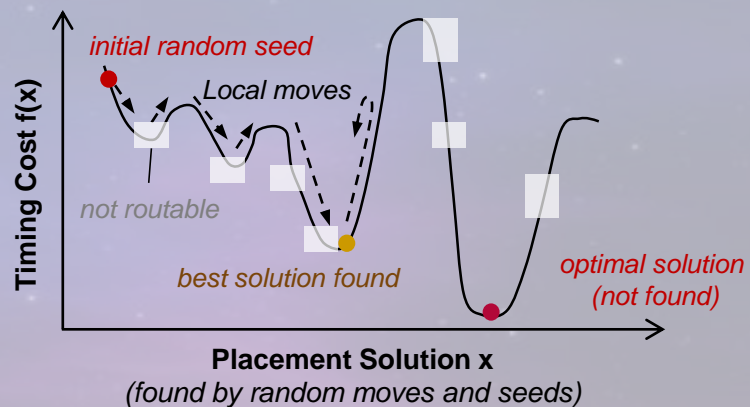
- Higher utilization enabled by routing
- Shorter net delays for performance
- Less wire switching for lower power



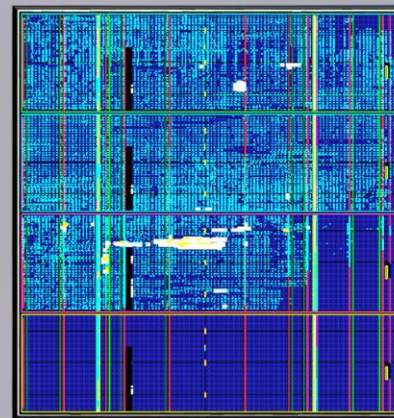
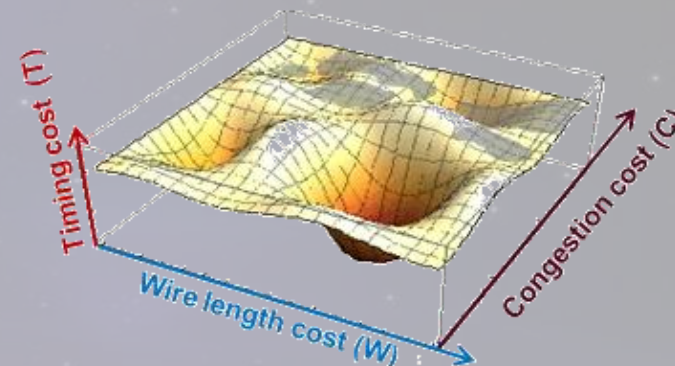
Vivado Design Suite Enables the UltraScale Advantage

Next Generation Implementation

ISE Design Suite (simulated annealing)

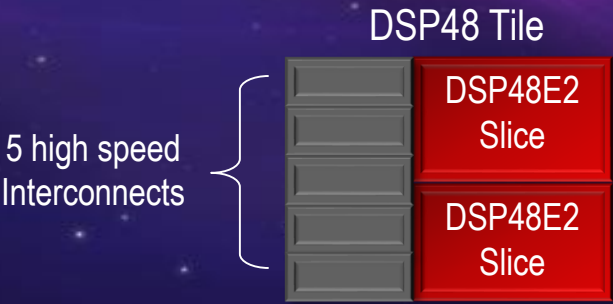


Vivado Design Suite (Analytical Placer)

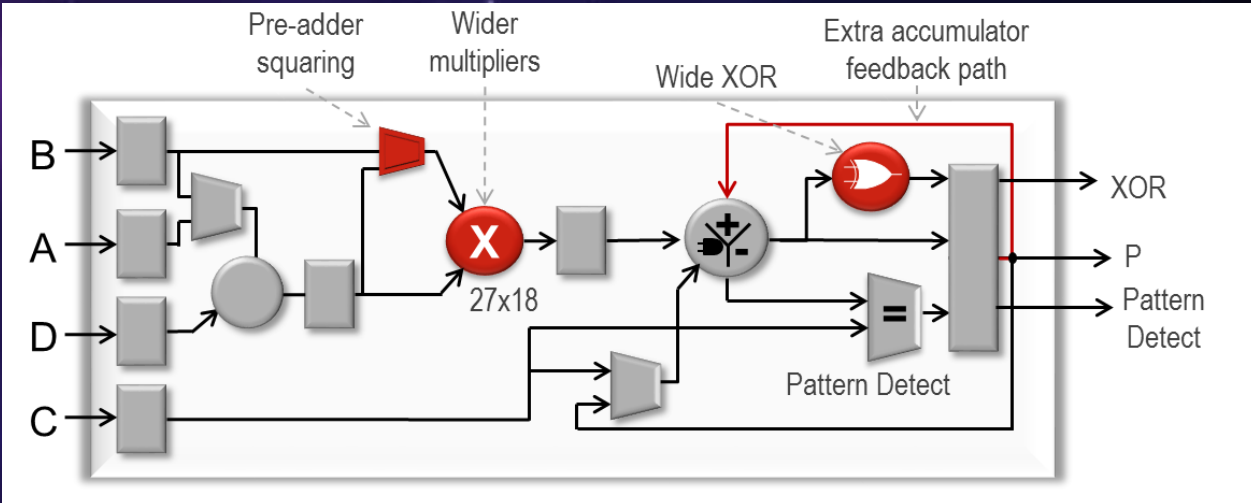


Enhanced DSP Sub-Systems for Performance and Efficiency

Feature	Benefit
27x18 multiplier in a DSP slice; 35x28 support in a DSP tile (2 slices)	<ul style="list-style-type: none">Optimal performance per blockImplement double-precision floating point in two-thirds the fabric
Pre-adder squaring	<ul style="list-style-type: none">More efficient motion estimation in video applicationsPerform “sum-of-square-difference” calculations in 50% fewer resources
Extra accumulator feedback path	Implement complex multiply-accumulate in half the resources
Wide XOR	Implement EFEC, CRC, ECC functionality
White box modeling	Full visibility with accurate simulation and debug

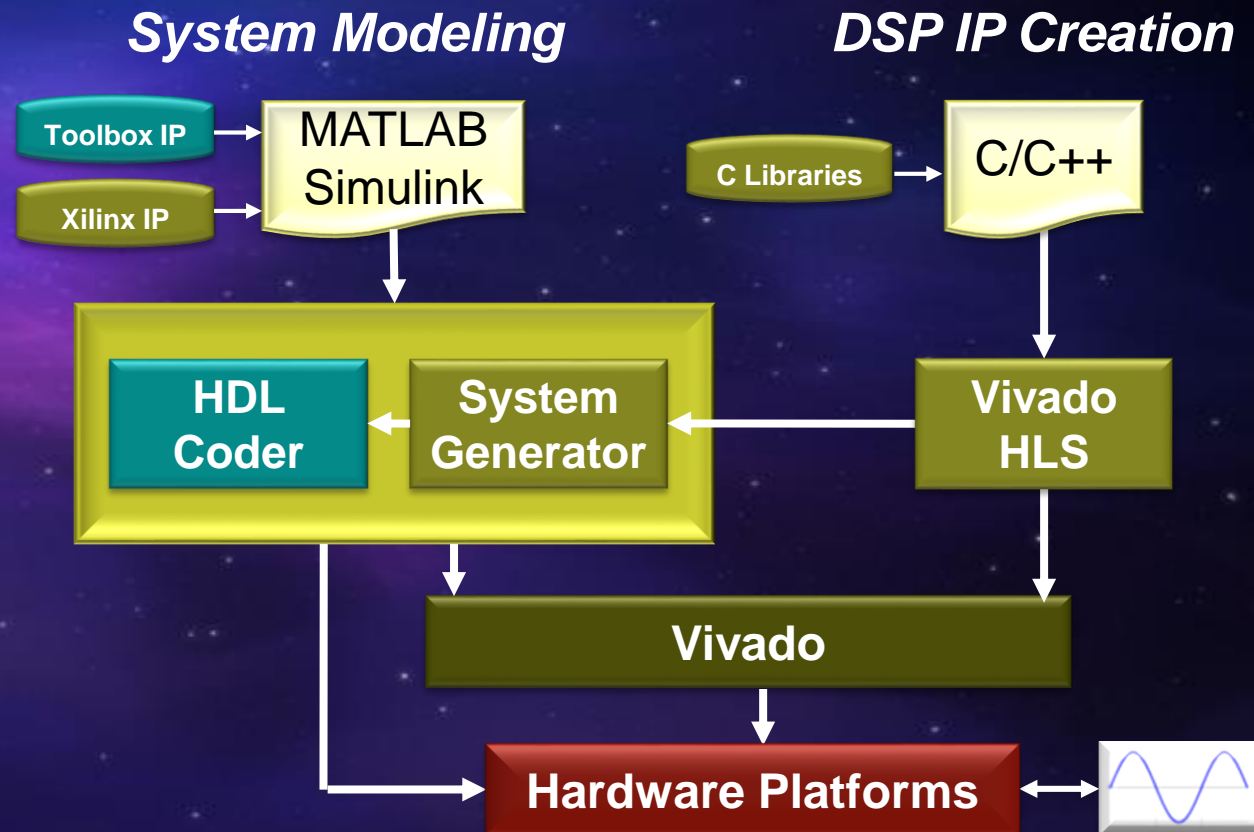


DSP Slice



Xilinx DSP Design Flow

- Floating-point and Fixed-point Hardware Generation
- World class C/C++ design flow
- Real time analog data acquisition



Vivado High-Level Synthesis: Accelerated IP Development and Design Space Exploration

➤ Comprehensive coverage

- C, C++, SystemC
- Arbitrary precision
- Floating-point

➤ Accelerated verification

- Magnitudes of order (2-3) faster than RTL for large blocks

➤ Fast compilation and design exploration

- Algorithm feasibility
- Architecture Iteration

➤ Customer proven results

Performance Estimates

Summary of timing analysis

Estimated clock period (ns): 2.74

Summary of overall latency (clock cycles)

Best-case latency: 18

Average-case latency: 18

Worst-case latency: 18

Latency interval (II): 1

Depth: 19

Area Estimates

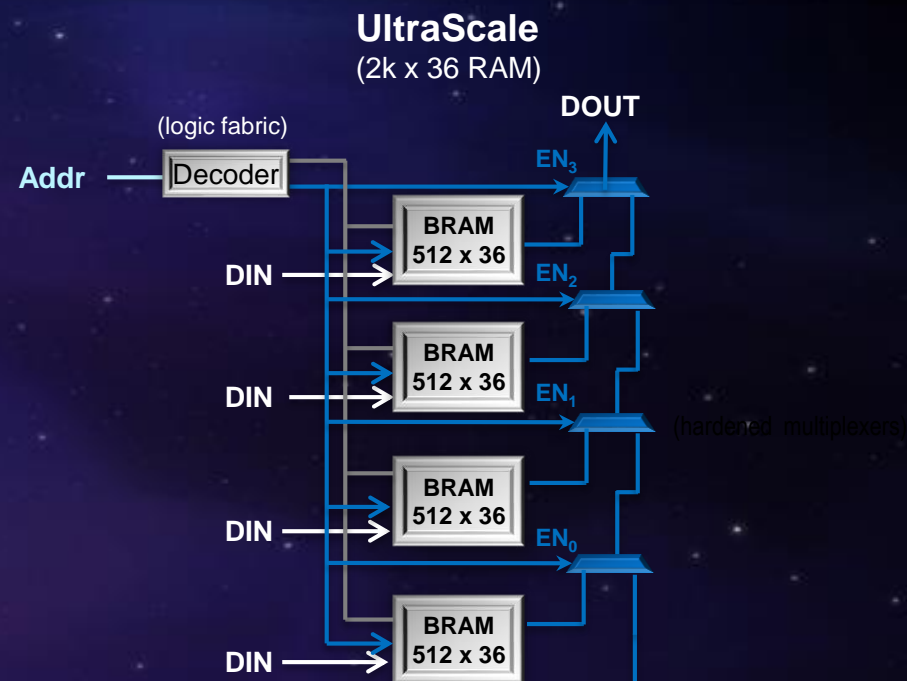
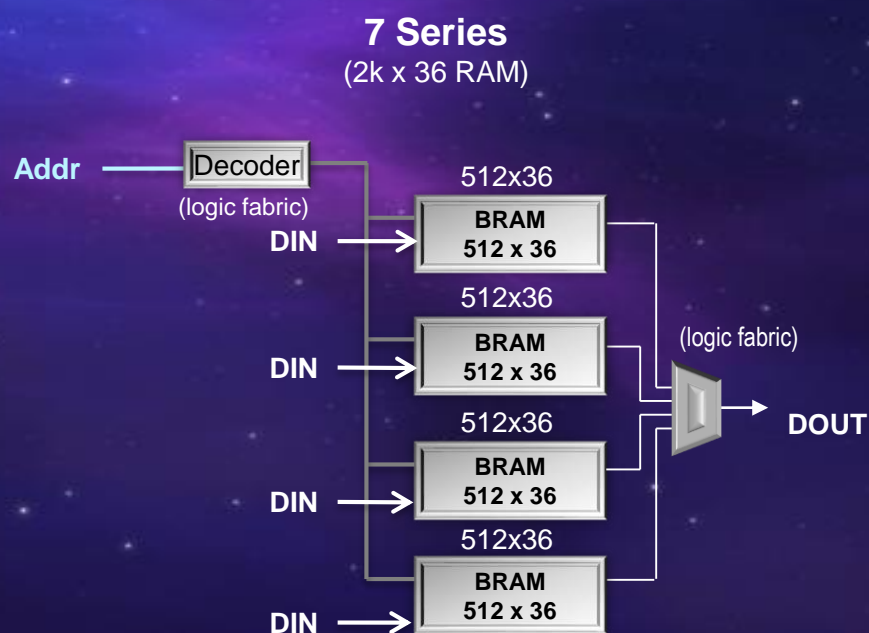
Summary

Component	BRAM	DSP48E	FF	LUT	SLICE
Expression	-	8	146	8	-
FIFO	-	-	0	739	-
Memory	11	-	-	-	-
Multiplexer	-	-	18	28	-
Register	-	-	-	-	-
Total	11	-	1619	-	-

	Hand-coded RTL	Vivado HLS
Design Time (weeks)	12	1
Latency (ms)	37	21
Memory (RAMB18E1)	134 (16%)	10 (1%)
Memory (RAMB36E1)	273 (65%)	138 (33%)
Registers	29686 (9%)	14263 (4%)
LUTs	28152 (18%)	24257 (16%)

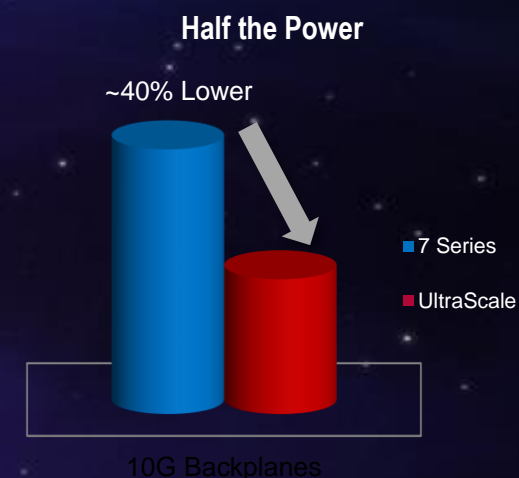
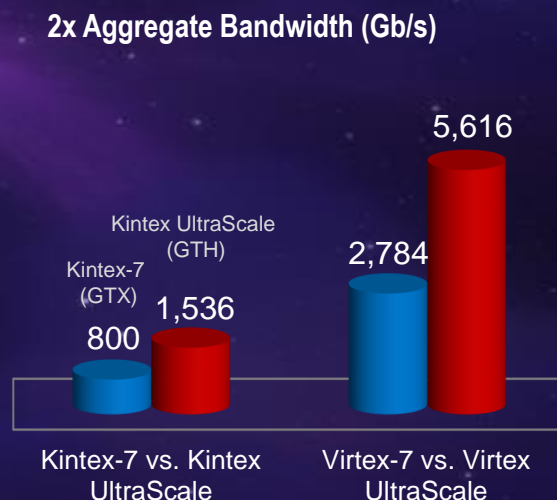
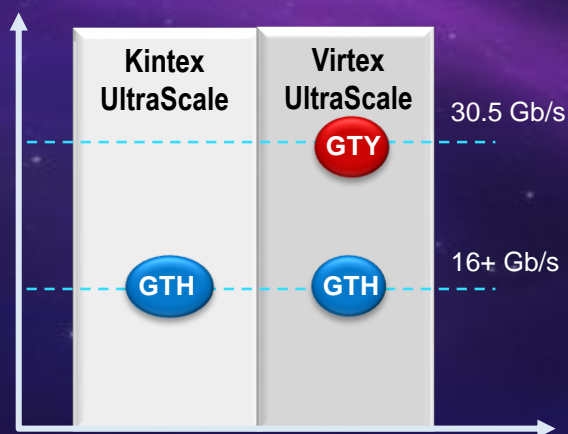
Optimized Block RAM Alleviate Bottlenecks for Many Applications

Feature	Benefit
Built in high speed memory cascading	Eliminates CLB usage, reduces routing congestion & dynamic power consumption
Enhanced FIFO	<ul style="list-style-type: none"> • Lower power, greater performance than soft FIFO • Easy migration to soft core implementation for additional functionality • Asymmetric read and write port widths for clock domain crossings
User-accessible power gating of active BRAM	Reduces dynamic power when access to BRAM contents is temporarily not needed

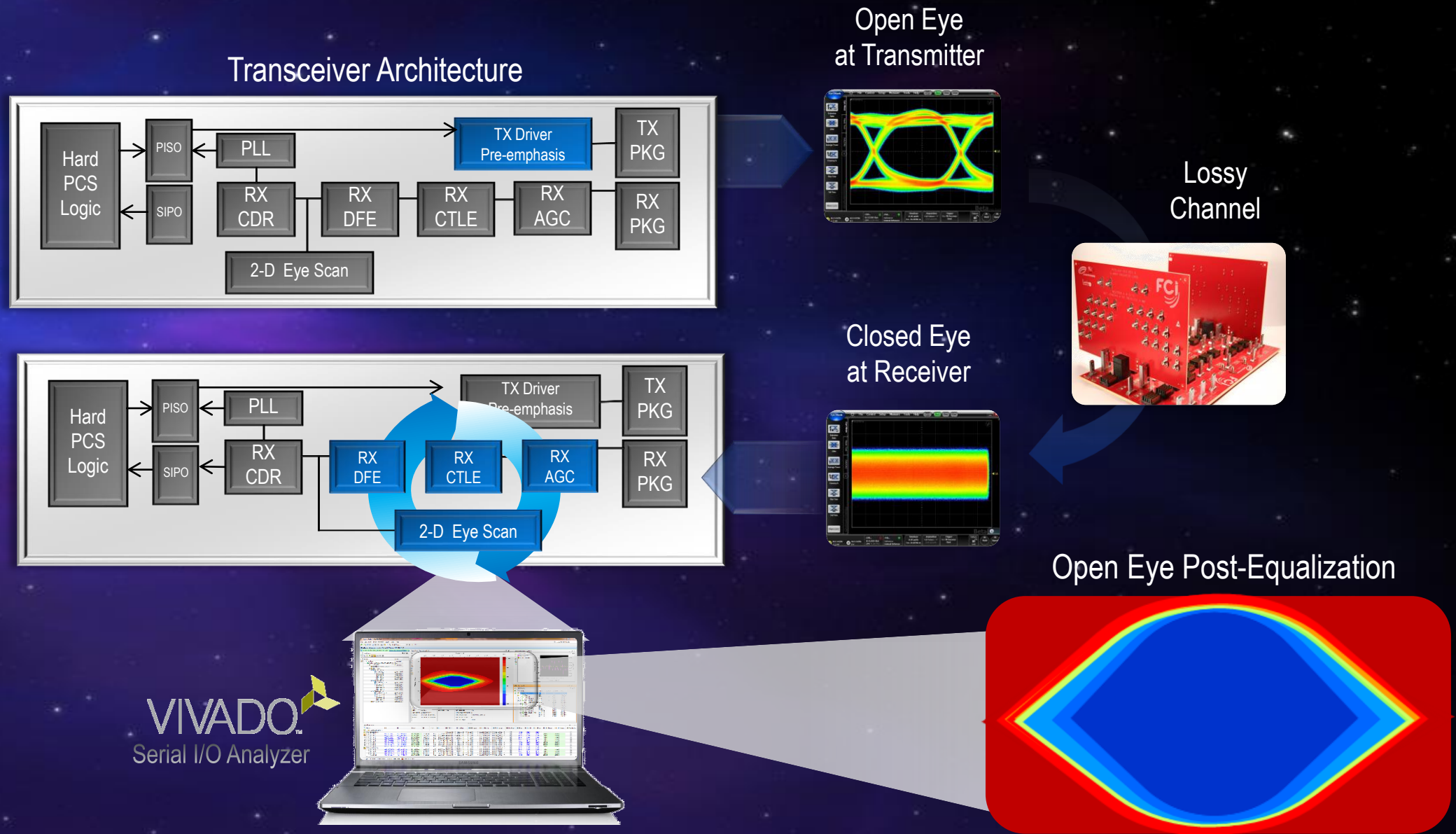


Delivering Massive I/O Serial Bandwidth

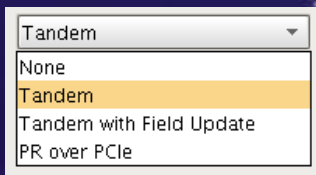
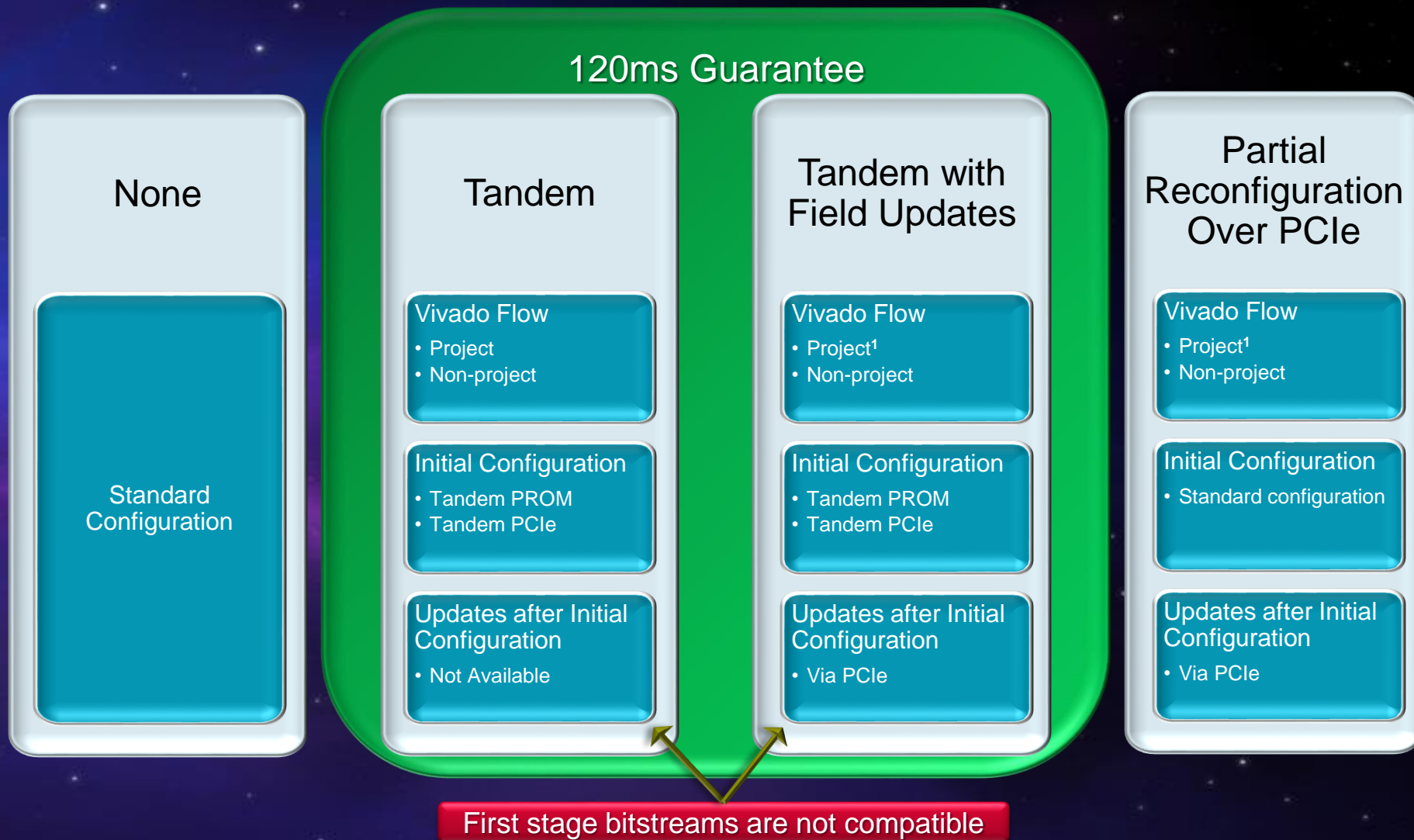
Feature	Benefit
GTH	<ul style="list-style-type: none"> 12.5Gb/s performance in -1 Speed and Military Temperature Grade Enabled Standards: <ul style="list-style-type: none"> PCIe Gen3 JESD204B Xilinx Aurora Serial RapidIO (SRIO) – Space VPX (VITA 78) / Next Generation Space Interconnect Standard (NGSIS) <ul style="list-style-type: none"> NGSIS IP Core from Alliance Program Partner, Praesum Supercomputing, developed on UltraScale Architecture
Major power reduction	~40% lower power over 7-Series for 10G backplanes
Continuous auto-adaptive equalization	Continuously optimizes link margin over PVT in increasingly challenging channel conditions



Auto-Adaptive Receiver Equalization in Action



UltraScale Configuration Options for PCIe



1: See Vivado Design Suite User Guide Partial Reconfiguration ([UG909](#)) for Project mode details

UltraScale Documentation

➤ [DS890](#) Architecture and Product Overview

➤ [DS892](#) Kintex UltraScale FPGAs Data Sheet

➤ White Papers

- [WP434](#) Xilinx UltraScale Architecture for High-Performance, Smarter Systems
- [WP446](#) Comprehensive JESD204B Solution Accelerates and Simplifies Development
- [WP451](#) UltraScale Architecture Low Power Technology Overview
- [WP454](#) High-Performance, Lower-Power Memory Interfaces with the UltraScale Architecture
- [WP458](#) Leveraging UltraScale Architecture Transceivers for High-Speed Serial I/O Connectivity

➤ User Guides

[UG570](#) UltraScale Architecture Configuration

[UG571](#) UltraScale Architecture SelectIO

[UG572](#) UltraScale Architecture Clocking Resources

[UG573](#) UltraScale Architecture Memory Resources

[UG574](#) UltraScale Architecture CLB

[UG575](#) UltraScale and UltraScale+ FPGAs Packaging and Pinouts

[UG576](#) UltraScale Architecture GTH Transceivers

[UG579](#) UltraScale Architecture DSP Slice

[UG580](#) UltraScale Architecture System Monitor

[UG583](#) UltraScale Architecture PCB Design

➤ Product Guides

- [PG150](#) UltraScale Architecture-Based FPGAs Memory Interface Solutions
- [PG156](#) UltraScale Devices Gen3 Integrated Block for PCI Express
- [PG182](#) UltraScale FPGAs Transceivers Wizard

MicroBlaze Triple Modular Redundancy (TMR) Subsystem

Micro-controller systems

➤ MicroBlaze TMR Fundamentals

- Triplication (TMR) for Fail Tolerant–Fail Safe (FT-FS)
 - First failure; continue nominal operation without degradation
 - Second failure; detect failure and halt operation
- Duplication (Lockstep) for Fail-Safe (FS)
 - **First failure; detect failure and halt operation**

➤ Triplicate MicroBlaze sub-system

- Voting at boundary
- Recovery of failing CPU under SW control (seen by application as servicing interrupt)

➤ Derived from MicroBlaze TMR designed for Zynq Ultrascale+ MPSoC (PMU & CSU)

- Add redundancy to detect failures and recover from faults without disrupting application
- Use Vivado IP Integrator to automate creation of a TMR system using handful of new IPs
- Partitioning into IP building blocks with automated triplication in Vivado

➤ MicroBlaze Triple Modular Redundancy (TMR) Subsystem v1.0 Product Guide

- https://www.xilinx.com/support/documentation/ip_documentation/tmr/v1_0/pg268-tmr.pdf

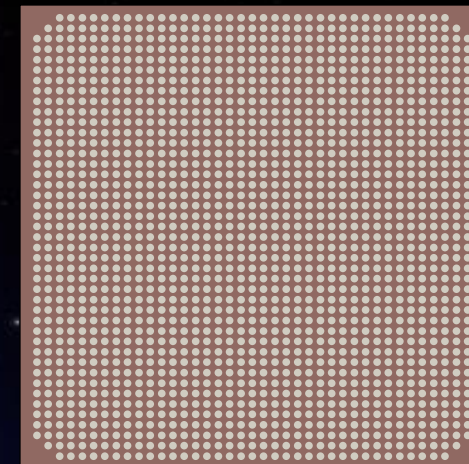
Space (XQR) Kintex UltraScale Product

➤ Packaged in 40mm x 40mm Ceramic Column Grid Array (CCGA)

- XQRKU060-CNA1509 Footprint compatible with commercial A1517 pin out
- Ceramic package loses 2 additional solder columns in each corner (1 XCVR & 4 HP/IO lost)

➤ Kintex UltraScale Advantage for Space Applications

- Deploys same commercial silicon mask set and 20nm wafer processing
- Vivado Ultrafast Development Advantage
 - [High Level Synthesis \(HLS\)](#)
 - [Block-based IP Integration with Vivado IP Integrator](#)
 - [Accelerated design implementation achieved through analytical place and route technology](#)
- Radiation Feasibility test data indicates XQRKU060 will meet Space customer needs – no need for RHBD re-design
 - NASA [Testing](#) showed no SEL up to 40 MeV-cm²/mg on Kintex UltraScale parts
 - Sandia National Laboratories testing showed no Single Event Latch-up (SEL) up to 79.2 MeV-cm²/mg
 - ★ “Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation”
<http://ieeexplore.ieee.org/document/7336736/>
 - ★ “An Analysis of High-Current Events Observed on Xilinx 7-Series and Ultrascale Field-Programmable Gate Arrays”
<http://ieeexplore.ieee.org/document/7891703/>
 - Xilinx testing on Kintex UltraScale
 - ★ No SEL susceptibility seen in testing up to 58 MeV-cm²/mg
 - ★ X-Ray Total Ionizing Dose (TID) test results good in testing up to 100 Krad

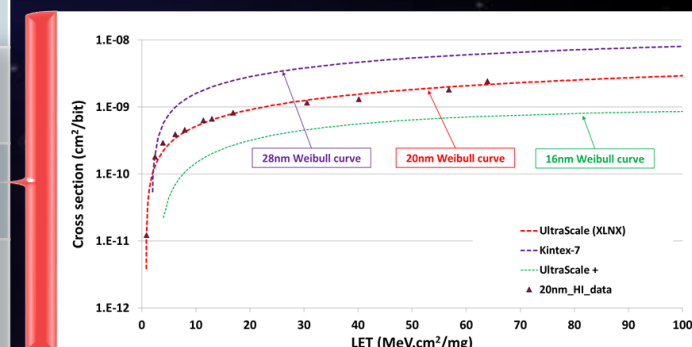


V5QV vs. XQRKU060-Using Commercial Die

	V5QV (SIRF)	XQRKU060
RadHard by Design	YES	NO
Silicon Modifications	YES	NO
Software Overlay Required	YES	NO
Special EPI Wafers	YES	NO
Ceramic Package	YES	YES
Space Test Flow	YES	YES
SEU Performance	Outstanding	Acceptable
SEL Performance	Outstanding (100 MeV-cm ² /mg)	Acceptable (79.2 MeV-cm ² /mg)
TID Performance	Outstanding (1 MRad)	Acceptable (100 KRad)



Cosmo Skymed NextGen



Next Generation Xilinx Space Product XQRKU060-CNA1509

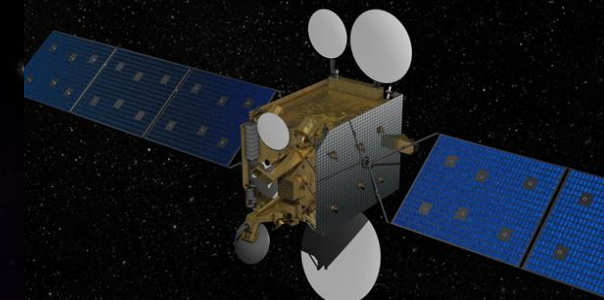
Space Product (XQR) Plan of Record Kintex® UltraScale™ FPGA

	Device Name	XQRKU060	
Logic Resources	System Logic Cells (K)	726	
	CLB Flip-Flops	663,360	
	CLB LUTs	331,680	
Memory Resources	Maximum Distributed RAM (Kb)	9,180	
	Block RAM/FIFO w/ECC (36Kb each)	1,080	
	Block RAM/FIFO (18Kb each)	2,160	
	Total Block RAM (Mb)	38	
Clock Resources	CMT (1 MMCM, 2 PLLs)	12	
	I/O DLL	48	
I/O Resources	Maximum Single-Ended HP I/Os	520	
	Maximum Differential HP I/O Pairs	240	
	Maximum Single-Ended HR I/Os	104	
	Maximum Differential HR I/O Pairs	48	
Integrated IP Resources	DSP Slices	2,760	
	System Monitor	1	
	PCIe® Gen1/2/3	3	
	Interlaken	0	
	100G Ethernet	0	
	12.5Gb/s Transceivers (GTH)	32	
Temp/Speed Grade	Military (-55°C to +125°C)	-1	
	Package Footprint	Package Dimensions (mm)	HR I/O, HP I/O, GTH
Prototyping Package	A1517	40x40	104, 520, 32
Flight Package	CNA1509	40x40	104, 516, 31



Product Table

Preliminary XQRKU060-CNA1509 Schedule



DLR H2 Communication Satellite

➤ Early programs may proceed directly to development

- Pin compatible commercial XCKU060/A1517 device available now!
- Target XCKU060/A1517 (-1 Speed Grade) in Vivado software
- Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit (XCKU040-2FFVA1156E) available now for \$2,995
 - Plan for Kintex UltraScale Space development kit later in 2018
 - ★ Will be possible to mount either XC or XQR part on Space Development board
 - ★ Similar to KCU105 board – customer inputs wanted now on board capabilities

➤ Flight Part Schedule

- | | |
|-----------------|---|
| – April 2018 | – Package Design Release |
| – October 2018 | – All piece parts available to begin assembly and test of qualification units |
| – December 2018 | – Pre-qualification Ready (Operations Space Test Flow hardware and procedures) |
| – June 2019 | – Complete pre-qualification validation with full qualification unit quantities |
| – December 2019 | – “B” Availability XQRKU060-CNA1509B |
| – December 2020 | – “Y” Availability XQRKU060-CNA1509Y |



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Thank You for your time

Space Policy for non-XQR Parts

It is the stated policy of Xilinx to only provide radiation performance data, guidance or support for the use of Xilinx products in Space Radiation Environment applications for products designated as Xilinx Space (XQR) products. As such, Xilinx will not provide this type of data, guidance or support for non-XQR products. The Space Radiation Environment is a branch of astronautics, aerospace engineering and space physics that seeks to understand and address conditions existing in space that affect the design and operation of spacecraft, launch vehicles and associated electronic systems. Only Xilinx Space (XQR) products are specified and endorsed for use in the space environment. The Xilinx standard terms and conditions state that the Xilinx Limited Warranty does not apply to and excludes to the maximum extent permitted by applicable law “Products used in an application or environment that is not within the Specifications”. Customers choosing to use Xilinx products in space environments that are not specified for use in space do so entirely at their own risk.

Xilinx continues to support the Xilinx Radiation Test Consortium weekly conference calls and annual meeting. Xilinx does post their proceedings from their annual meeting in our Xilinx Space Lounge by prior agreement with the Consortium. Do note that the XRTC is a distinct and separate organization from Xilinx. The current chairperson for the XRTC is Gary Swift, who can be contacted via the information below:

Swift Engineering and Radiation Services, LLC

408-628-4803 (landline) or 408-679-3785 (cell)

Email: gary.m.swift@ieee.org